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10/039,961	12/31/2001	Andrew F. Glew	P13736	8435
59796 7590 07/12/2010 INTEL CORPORATION c/o CPA Global P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER PYZOCHA, MICHAEL J	
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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/039,961  
Filing Date: December 31, 2001  
Appellant(s): GLEW ET AL.

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Thomas R. Lane  
(Reg. No. 42,781)  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 05/12/2010 appealing from the Office action mailed 06/03/2008.

**(1) Real Party in Interest**

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The following is a list of claims that are rejected and pending in the application:

1, 2, 4-6, 8, 9, 12-18, 22 and 23

**(4) Status of Amendments After Final**

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

**(5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

**(7) Claims Appendix**

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

**(8) Evidence Relied Upon**

US 6651171 B1	ENGLAND et al.	11-2003
US 6704872 B1	OKADA	03-2004
US 20030037237 A1	ABGRALL et al.	02-2003

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**Claim Rejections - 35 USC § 103**

Claims 1, 2, 4-6, 8, 9, 12-14, 16-18, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. (US 6651171) in view of Okada (US 6704872).

As per claims 1 and 23, England et al. discloses a processor comprising: memory; one or more execution units loading an authenticated code module into the memory, locking the memory (see column 6 lines 5-39 and 47-67), retrieving a key, authenticating the authenticated code module stored in the memory using the key, and initiate execution of the authenticated code module stored in the memory (see column 3 lines 35-43; column 3 line 65 through column 4 line 13 and column 13 lines 15-26).

England fails to explicitly disclose decode logic to receive a launch instruction and the one or more execution units to execute the launch instruction by loading an authentication code.

However, Okada teaches decode logic to receive a launch instruction (see column 4 lines 31-52) and the one or more execution units to execute the launch instruction by loading an authentication code (see column 10 lines 41-64).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the execution method of Okada in the England et al. system.

Motivation to do so would have been to provide a processor having a function to prevent the illegal execution of a program (see Okada column 4 lines 31-32).

As per claim 2, the modified England et al. and Okada system discloses a cache memory that provides the memory (see England et al. column 8 lines 21-25).

As per claims 4-5, the modified England et al. and Okada system discloses the execution units lock the cache memory to prevent replacement of lines of the authenticated code module stored in the cache memory (see England et al. column 7 lines 1-4 and column 11 lines 40-63).

As per claims 6 and 22, the modified England et al. and Okada system discloses a decoder to generate one or more opcodes for the launch instruction, wherein the execution units authenticate and execute the authenticated code module in response to executing the one or more opcodes (see England et al. column 9 lines 5-19).

As per claims 8, 9, and 12-14, the modified England et al. and Okada system discloses a key, wherein the execution units utilize the key to authenticate the

authenticated code module and wherein the execution units, in response to the launch instruction retrieve a key from a chipset and use the key to authenticate the authenticated code module stored in the memory (see England et al. column 13 lines 10-62 and column 15 lines 19-52).

As per claims 16-18, the modified England et al. and Okada system discloses the execution units initiate execution of the authenticated code module only if the authenticated code module is determined to be authentic (see England et al. column 9 lines 12-15 and column 7 lines 35-59).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified England et al. and Okada system, as applied to claim 1, in view Abgrall (US 20030037237).

As per claim 15, the modified England et al. and Okada system fails to the use of RSA and SHA-1 for the digital signature verification. However, Abgrall discloses that RSA and SHA-1 are commonly used in signature verification (see paragraph 346).

It would have been obvious to one of ordinary skill in the art at the time the invention to combine the ideas of Abgrall with those of the modified England et al. and Okada system.

Motivation to do so would have been that RSA and SHA-1 are commonly used and known to be effective algorithms for use in such a verification process.

**(10) Response to Argument**

Appellant argues (see Brief page 9) with respect to claim 1 that the combination of England and Okada is improper because there is no motivation to combine the references.

With respect to this argument it is noted that Appellant states, "Combining Okada and England would do nothing to help Okada prevent the illegal execution of a program", however, Okada was combined with England such that the Okada reference modifies the England reference. Appellant also states that this combination would "not help England hide the execution of curtailed code from the normal operation of a system", however, the combination was put forth to improve the hiding the execution of curtailed code of England. In response to Appellant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). As Appellant states England allows all programs to legally or illegally execute, and in this case, the relied upon sections of Okada give the added benefit of preventing

the illegal execution of a program. One of ordinary skill in the art would recognize that preventing illegal execution of a program increases the security of the system thereby providing reason to combine Okada with England. Therefore, there is motivation to combine Okada with England and this combination is proper.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Michael Pyzocha/

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Conferees:

/Emmanuel L. Moise/  
Supervisory Patent Examiner, Art Unit 2437

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